Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.An analog to digital converter (ADC) comprising:
at least one folder receiving an input voltage, generating a first output voltage and a second output voltage, and including:
a plurality of amplifiers, wherein each of the amplifier receives one of a plurality of reference voltages and comprises:
a bias circuit for providing a bias current to the amplifier based on at least one of a plurality of bias control signals; and
calibration logic for generating the bias control signals according to the first output voltage and the second output voltage;
wherein during calibration, the calibration logic provides the bias control signals to control the bias circuit of each amplifier in the folder such that the first output voltage is substantially the same as the second output voltage.

[c2] 2.The ADC of claim 1, wherein each amplifier further comprises:
a first transistor having a gate to receive one of a plurality of reference voltages, a drain to output the first out-

put voltage, and a source;

a second transistor having a gate to receive the input voltage, a drain to output the second output voltage, and a source; and

an impedance coupled between the source of the first transistor and the second transistor; and

wherein the bias circuit further comprises:

a first bias circuit coupled to the source of the first transistor for drawing a first bias current of the first transistor; and

a second bias circuit coupled to the source of the second transistor for drawing a second bias current of the second transistor.

[c3] 3.The ADC of claim 2, further comprising:

a first multiplexer for selectively setting the input voltage to substantially the same potential as one of the reference voltages according to a reference control signal;

wherein the calibration logic further generates the reference control signal; and

wherein during calibration, for each amplifier in each folder, the calibration logic sets the input voltage substantially the same as the reference voltage for the amplifier using the reference control signal.

[c4] 4.The ADC of claim 2, wherein the impedance is a resistor.

[c5] 5.The ADC of claim 2, wherein the sum of the first bias current and the second bias current is constant.

[c6] 6.The ADC of claim 1, wherein during calibration, for each amplifier in each folder, the first bias current and the second bias current are adjusted by a predetermined amount using at least one of the bias control signals.

[c7] 7.The ADC of claim 6, wherein during calibration, for each amplifier in each folder, the calibration logic iteratively adjusts the value of the first and the second bias current of the amplifier, wherein the adjustment is iterated i times and the predetermined amount is Bmiddle / 2^{i+1} wherein Bmiddle is half of the sum of the first and the second bias current.

[c8] 8.A method of calibrating an analog to digital converter (ADC) having at least one folder receiving an input voltage, generating a first output voltage and a second output voltage, and including a plurality of amplifiers, each amplifier is for receiving one of a plurality of reference voltages; wherein, for each amplifier in each folder, the method comprises the following steps:
setting the input voltage to be substantially the same as the reference voltage corresponding to the amplifier; and
adjusting at least one of the bias currents of the ampli-

fier based on the first and the second output voltage such that the first output voltage is substantially the same as the second output voltage.

[c9] 9.The method of claim 8, wherein for each of the amplifiers in each folder, the bias currents further include first and second bias currents, wherein when adjusting the bias currents of the amplifier, the sum of the first and the second bias currents is constant.

[c10] 10.The method of claim 9, wherein adjusting the first and the second bias currents further comprises the following steps:
setting the first bias current and the second bias current to be half of the sum of the first and the second bias current;
sampling the first output voltage and the second output voltage; and
adjusting the first and the second bias currents based on the first and the second output voltages, wherein the first output voltage corresponds to the first bias current and the second output voltage corresponds to the second bias current.

[c11] 11.The method of claim 10, wherein the first and the second bias currents are adjusted by a predetermined amount.

[c12] 12. The method of claim 11, wherein the first and the second bias currents are iteratively adjusted by the pre-determined amount for i times, and the predetermined amount is Bmiddle / 2^{i+1} , wherein Bmiddle is half of the sum of the first and the second bias current.